Amendments to the Claims

Please cancel claim 11, amend claims 1, 4, 5 and 7, and add new claim 12 as shown in the following listing of claims. This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (currently amended) An electronic device comprising a transistor provided at a surface of a semiconductor substrate, the transistor having a source and a drain that are mutually connected through a channel, which transistor is further provided with a gate electrode for influencing an electron distribution in the channel and with a shield present between the gate and the drain, which drain is provided with a drain extension extending in the substrate towards the channel, the drain having a contact, said drain contact and said gate being mutually separated through an extension area, wherein the shield has a two-stepped structure in the extension area comprising a first step and a second step, the first step and the second step having a combined height shorter than a height of the gate electrode ~~each of the first step and the second step having a height not substantially less than a thickness of said shield~~.

2. (previously presented) An electronic device as claimed in claim 1, wherein a L-shaped spacer is present between the gate-electrode and the shield.

3. (previously presented) An electronic device as claimed in claim 1, wherein the shield is formed as a metal silicide.

4. (currently amended) An electronic device as claimed in claim 1, wherein the drain extension is provided with a first and a second region, the first region having interfaces with the channel and the second region, the second region having an interface with a contact area within the drain, which first region has a higher dopant concentration than the second region, and wherein the first region is ~~substantially~~ present within a shield area defined by a perpendicular projection of the shield on the substrate.

5. (withdrawn-currently amended) An electronic device comprising a transistor provided at a surface of a semiconductor substrate, the transistor having a source and a drain that are mutually connected through a channel, a source electrode, and a drain electrode, which transistor is further provided with a gate electrode for influencing an electron distribution in the channel and with a shield, separate from the source electrode, present between the gate and the drain, which drain is provided with a drain extension extending in the substrate towards the channel, the drain having a contact, said drain contact and said gate being mutually separated through an extension area, ~~area ,~~ which drain extension is provided with a first and a second region, ~~region ,~~ the first region having interfaces with the channel and the second region, ~~region ,~~ the second region having an interface with a contact region within the drain, wherein the first region has a higher dopant concentration than the second region, and the first region is substantially present within a shield area defined by a perpendicular projection of the shield on the substrate.

6. (previously presented) An electronic device as claimed in claim 4, wherein the interface between the first and the second region is present within the shield area.

7. (currently amended) An electronic device as claimed in claim 4, wherein a ~~the~~ ratio of the dopant concentrations in the first and the second region is in the range of 1.2 to 2.5.

8. (withdrawn) An electronic device as claimed in claim 5, wherein the shield is electrically connected to the source through an electrical connection.

9. (withdrawn) An electronic device as claimed in claim 8, wherein the electrical connection comprises a capacitor.

10. (previously presented) An electronic device as claimed in claim 1, wherein the semiconductor substrate is made of silicon and the transistor is of the LDMOS type.

11. (canceled).

12. (new) An electronic device as claimed in claim 1, wherein the first step and the second step are situated such that an upper surface of each of the first and second steps is located a level closer to the semiconductor substrate than an upper surface of the gate electrode.